A Novel Architecture for Quantum-Dot Cellular ROM

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Abstract— **Quantum-dot cellular automata (QCA) offers a novel alternative to the transistor paradigm. Matching architecture to QCA device characteristics is of high importance and failure to do so may squander potential gains. In this paper a new architecture for quantum-dot cellular ROM (QCROM) has been proposed. The presented architecture could raise the total storage density of QCA storage devices to about 250Gb/cm².**

I. INTRODUCTION

It is obvious that with current advances in the digital communication algorithms, protocols and systems, related to the bandwidth-hungry digital data, there is a vital need for advanced devices and circuits from the viewpoint of speed, size and power consumption. Conventional semiconductor-based integrated memories have been developed so far to store information via current switches in the form of electronic charge state. Consider a current switch i.e. a transistor in CMOS technology with an average footprint a operating at frequency f moves N_e electron in each clock cycle from power supply (V_{dd}) to ground through the channel. Each electron transiting the channel dissipates energy $eVdd$. The dissipated power density is then $P=N_efeVdd/a$ watts/cm². Even with $a=100nm^2$ (10^{12} devices/cm²), a supply voltage of $Vdd=0.1V$, $f=100GHz$, and $Ne=10$, the power dissipation will still be $16kW/cm^2$. This analysis holds no matter how the transistor is made [1]. From the viewpoint of density, exploiting CMOS current switches in designing digital data storage there are also challenging limitations. Typical NAND ROMs use cell size of $4F^2$, where F stands for feature size of the used technology. That is to say exploiting 0.25μm process technology parameters, storing one digital bit requires area of about $0.25\mu m^2$; yielding density of $400MBit/cm^2$.

The seemingly development in microelectronics has been the consequence of industry's ability to continuously scale down the transistor. Obviously the Moor's law cannot continue for microelectronic device manufacturing forever. The leakage currents through the gate oxide resulting from quantum mechanical tunneling of electrons from the gate electrode through the oxide and into transistor channel are one clear reason. As the size of transistors scale down, more and more of these quantum mechanical effects appear and affect the normal operation of transistors [2, 3]. Consequently, conventional microelectronics based on current switches has power consumption, density and frequency limitations. Thus, a new paradigm beyond current transistor switches is required.

The quantum-dot cellular automata has become the very promising technology for designing the new generation of digital embedded systems. QCA has made the computations possible to be carried out at nanoscale. Due to its basic theory and characteristics, including low power consumption, high density and the ability to work in high frequencies, it has attracted the attention of many scientists from all over the world. Moreover, the QCA potential for regularity makes it an attractive technology for manufacturing integrated digital systems.

QCA takes advantage of quantum mechanical effects such as electron tunneling at nanoscale. It was introduced by Lent et al in 1993 [4] and has recently become one of the promising candidate paradigms for nano-computing. A significant amount of theoretical and practical research has been done in this field [5-8].

Although QCA is still in research stages, some experimental nanoelectronic devices have been manufactured with expected functionality [8-10]. Several circuits based on the capabilities of the QCA have been proposed so far. Many of them take advantage of coplanar wire crossing which makes the design independent of metal layer interconnects.

We presented the functionality of a simple quantum-dot cellular ROM (QCROM) in [11] as a digital data storage. In this paper we will discuss another possible architecture and implementation which is more efficiently adapted to QCA logic and allows us to exploit the maximum possible density of the device to store information.

II. REVIEW OF QCA

A QCA cell consists of four quantum dots and two loaded electrons [7] as in Fig.1. Dots are places where the charge could be localized. The two electrons will tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. However, they can change their positions within dots as a result of tunneling effect. This phenomenon takes place when potential barrier that separates the dots is low. Consequently, two configurations are possible which can be used to encode binary information as in Fig.1.

When placing quantum cells adjacent to each other, due to the electrostatic force they will interact in the way that the polarization of one cell will be directly affected by the polarization of its neighboring cells. In this manner state can be propagated along a line of adjacent QCA cells, forming a wire. One can use an array of QCA cells as a wire to transmit information from one end to another as in Fig.2.
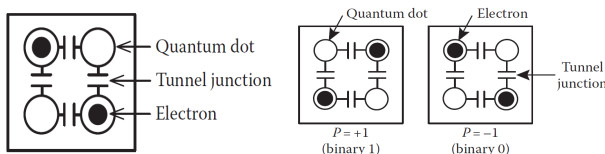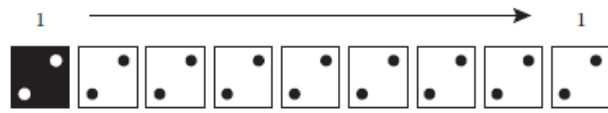
Figure 1. A quantum cell and binary encoding.

Figure 2. Transmitting information through a line of QCA cells.
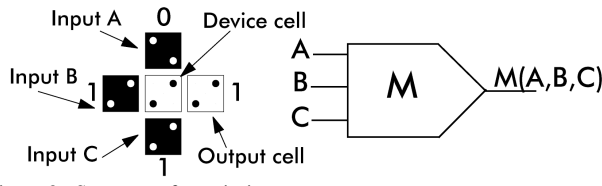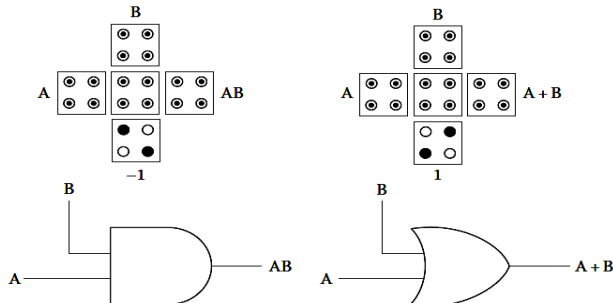

Figure 3. Structure of a majority gate.

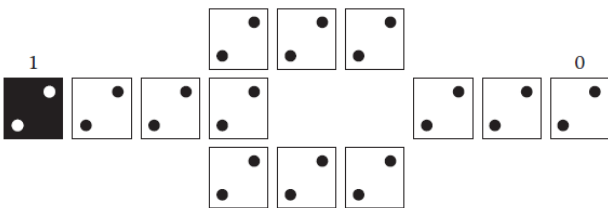Figure 4. Creating AND, OR gates from majority gate.
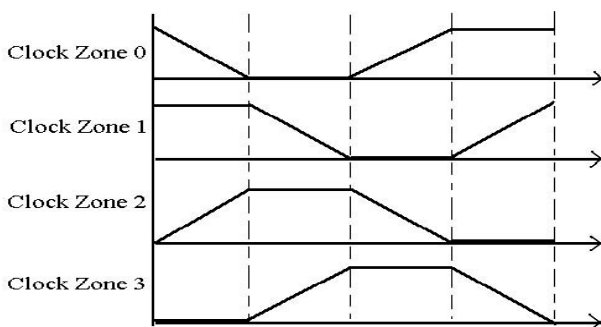

Figure 5. QCA NOT gate.

Figure 6. Clocking scheme of QCA circuits.

A very basic QCA gate is called majority gate as shown in Fig.3. We can easily prove that all other logical gates like AND, OR are implementable by majority gate [7, 12]. Fig.4 shows how AND, OR gates are created using Majority gate. Fig.5 also shows the structure of a NOT gate. One important thing about QCA information flow is the clocking scheme, that is to say, for adjacent cells in order to control the polarizations reactions and effects, one should hold the polarization of the first cell fixed and lower the potential barrier of its adjacent cell in order to

let the electrons of the adjacent cell relocate. This phenomenon should repeat over and over again to pass the information through line of cells. It has been shown that for a QCA circuit to function correctly, only four clocking zones are necessary. Each clock signal is lagging 90 degrees in phase with respect to the previous clocking [12, 13]. The four clock zones are shown in Fig. 6.

Coulombic interactions cause electrons to move within a cell, not between cells, so there is no current flow [14]. This avoids many of the heat dissipation and power consumption problems of transistor computing. Unlike CMOS, in QCA the transmission media and logical elements are both comprised of the same basic block- the cell. As such, QCA has been called "processing- in-wire"

QCA cells have been already implemented using metal island dots under low temperature [9], but an interesting possibility is the implementation of QCA cells on the molecular level [15]. By using single molecules as the cells, and regions within the molecule as sites for electrons, molecular QCA holds the promise of densities upwards of 10^{13} devices /cm^2. Clock speeds for these cells could be in the 1 to 10 Terahertz range at room temperature. Power consumption should be far less than end-of-line high performance transistors in CMOS.

III. QUANTUM-DOT CELLULAR ROM

A. Possible Architectures

Any digital data storage consists of two parts, namely, the storage part and the readout part. The readout part may consist of decoders, tri-state buffers, flip flops, etc. We have already presented the implementation of a single layer quantum-dot cellular ROM (QCROM) in [11]. With conventional QCA designing schemes there are two possibilities for implementation of QCROM. Taking advantage of coplanar wire crossing via exploiting 45 degree rotated cells, one can efficiently improve the storage density (bit/cm^2). Fig. 7 depicts a 4x4 QCROM implemented in four layers. Two via layers have been used to pass data between the main cell layer and cross contact layer. In this QCROM layout, the cell spacing is two while the radius of effect of each cell is 65 nanometer. It takes 1T (4ø$_i$ where each T state consists of four ø$_i$ states) for the decoder to activate the appropriate select of each bit cell, and 1ø$_i$ for each bit cell to make the bit available to the output terminal. As a next step the serial OR makes the bit available at the output data bus. This operation takes 1ø$_i$ in its turn. Therefore, it will take 9ø$_i$ for any bit in the last column to appear at the data terminal of the ROM.

Fig. 8 shows the same 4x4 QCROM implemented in one layer. Taking advantage of the 45 degree rotated cells, it is possible to cross wires in the same layer. Consequently, one can efficiently improve the storage density. However, in this case special consideration about the radius of effect and correct cell alignment should be taken into account. The capacity of this QCROM can be easily increased via using several layers on top of each other. The data bits are stored in the form of fixed polarity QCA cells.
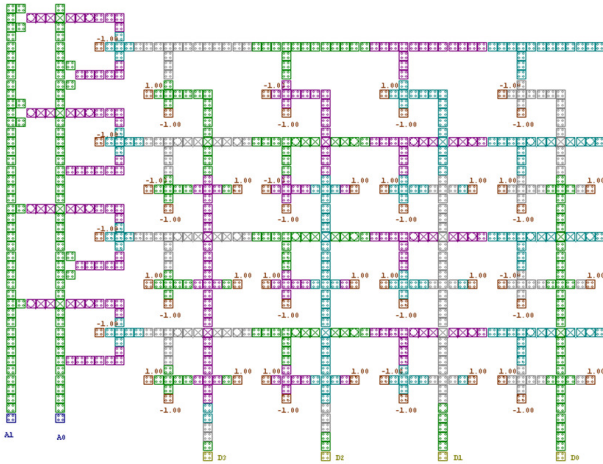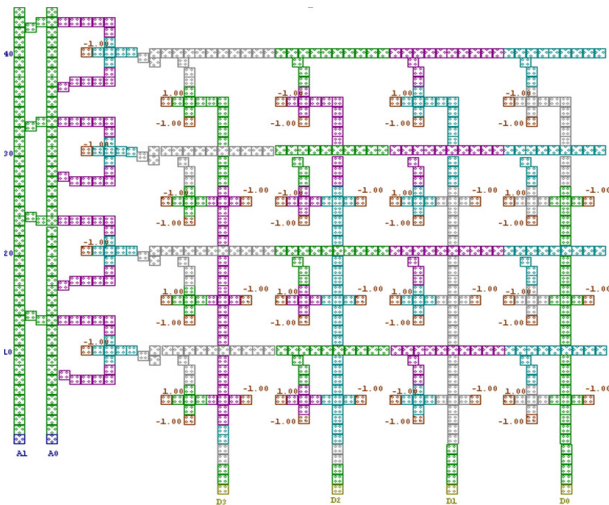
Figure 7. Layout of a four layer 4x4 QCROM.

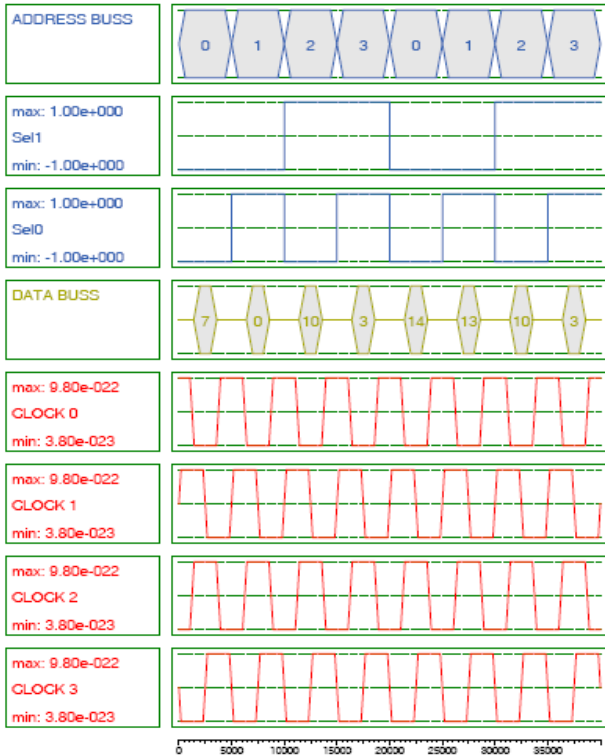Figure 8. Layout of a single layer 4x4 QCROM.

Figure 9. Simulation results of 4x4 QCROM.

TABLE 1.
QCA ROM CONTENTS

ADRESS (A_1A_0)	DATA ($D_3D_2D_1D_0$)
00	1010
01	0011
10	1110
11	1101

TABLE 2.
QCA ROM SPECIFICATIONS

ROM Type	QCA 4 Layer	QCA 1 Layer
Number of Cells	864	692
Access Time (T)	9/4	9/4
Area (μm^2)	1.19	1.10
Capacity (Gb/cm^2)	1.8	1.8

B. QCROM Simulation

The density matrix approach is used to manipulate the coherence vector simulation. It is used to model the dissipative effects and also perform a time-dependent simulation of the design [16]. It assumes each cell as a simple-state system. The following Hamiltonian is constructed for this two-state system;

$$H = \sum_j \begin{bmatrix} -\frac{1}{2} p_j E_{ij}^k & -\gamma_j \\ -\gamma_j & \frac{1}{2} p_j E_{ij}^k \end{bmatrix} \quad (1)$$

In this equation, E is the kink energy between cell i and j. This kink energy and the energy cost of two cells with opposite polarization are associated with each other. P_j represents the polarization of cell j and γ_j is the tunneling energy of electrons within the cell j which is directly related to the clock, i.e. the clock value is the tunneling energy. The summation is over all cells within an effective radius of cell i, and can be set prior to the simulation. With the aid of this Hamiltonian, Schrodinger time invariant equation can be written as following:

$$H_i \psi_i = E_i \psi_i \quad (2)$$

A solution to this equation that helps us to find the polarization of a cell will be [17]:

$$p_j = \frac{\frac{E_{ij}^k}{2\gamma} \sum_j P_j}{\sqrt{1 + \frac{E_{ij}^k}{2\gamma} \sum_j P_j}} \quad (3)$$

Table 1 shows the contents of each ROM in our simulation. Both coherence vector and bistable approximation methods have been exploited in QCAdesigner [17] CAD tool to simulate the QCROMs. The simulation results have been shown in Fig. 9. The specifications of these ROMS are in table 2.

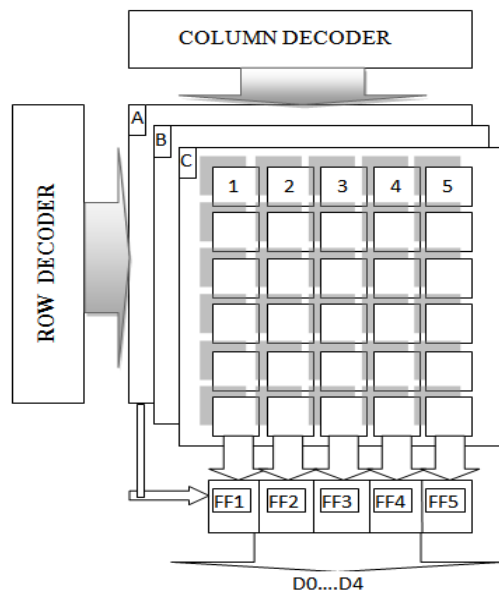Due to the operation of the QDCA cells in low voltages, a

Fig. 10. Architecture of the proposed QCROM.

transient noise in clocking scheme may lead to a change in the polarity of data cells in a very short period of time and consequently the read data is wrong. This is more likely to happen in QCA RAMs.

In order to design a more fault tolerant ROM, we suggest use two quantum dots in data cells. This reduces the risk of transient data cell polarity change. The challenges of current QCA technology include driving inputs and outputs of the circuit and temperature considerations.

C.   New QCROM architecture

It is seen that the readout circuitry implemented in QCA reduces the effective capacity of the layer in terms of fixed cells. For the previous architectures, the readout cells are about 70 percent of the used sells in designing QCROM. The readout circuits in previous QCROMs were the serial OR gate, decoder and bit select part. If one implements the readout circuit in another layer then there is a possibility to store all cells near each other in one layer. This in turn would result in a higher capacity. Consider the size of each cell is 18nmx18nm, with 2nm spacing between cells it is possible to store 250Gb of data in each square centimeter. The layout of such ROM has been shown in Fig. 10. This ROM consists of three layers, namely, the clocking layer (A), the main cell layer (B) where the stored data is kept and an extra layer to help with reading the data (C). Although the clocking scheme of these ROMs are a bit more complicated than previous ROMs, their high capacity is a motivation to fabricate them in this form. Two decoders named as row decoder and column decoder select the related bit cell based on the address. Each time the address is decoded, the sequence of n cells are energized (in Fig.10 n=5) one after each other. Suppose the address points to the first row. In this case the first cell is energized and consequently changes the polarization of the QCA wire in layer C. This wire is ends at a flip flop and via correct clocking scheme restores the bit in the flip flop. Then the

column decoder energizes the next cell in the same row and a similar scheme is repeated until the last bit is restored in the last flip flop.

IV.   CONCLUSION

New device paradigms require new system architectures. Architecture must enable the realization of the high functional densities and performance. In this paper we discussed and presented that conventional single layer and multilayer architectures reduce the possible high density of QCROMS in terms of readout circuits. To overcome this problem, a new architecture for QCROM was presented which would enable the storage density of about 250Gb/cm^2.

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